Application-Oriented Active Power Cycling of SiC MOSFET Power Modules with Multiple TSEP Acquisition

Kevin Muñoz Barón¹, Jeremy Nuzzo¹, Tobias Fink¹ and Ingmar Kallfass²*

¹Institute of Robust Power Semiconductor Systems, University of Stuttgart, Germany
²ingmar.kallfass@ilh.uni-stuttgart.de

Abstract

Multiple temperature-sensitive electrical parameters (TSEP) of 1.2 kV SiC MOSFET power modules are continuously measured online in the operation of a dynamic AC active power cycling test. The acquired TSEPs are threshold voltage, peak gate current and on-state resistance. A miniaturized TSEP acquisition board with microcontroller and isolated digital interface is designed to be directly stacked with the gate driver board and power module. A sample rate of 200 Sa/s is achieved at an averaging count of 100 for a PWN frequency of 20 kHz.

Introduction

With further advances in electric vehicles, more stringent requirements are being placed on the power electronics. Not only should they be efficient, but also reliable. Silicon carbide (SiC) based transistors can overcome the physical limits of silicon (Si)-based devices because of their intrinsic wide bandgap material properties. While this bodes well for the achievable efficiency, at the same time, reliability concerns for SiC power devices exist, especially at the SiO₂/SiC interface [1], [2]. Throughout the lifetime of a power device, multiple electrical parameters will change and can affect the operation of the converter or the device itself. These parameters are often measured in active power cycling tests (PCTs), where they are used for end-of-life (EOL) detection [3]. While this is possible in a conventional PCT scenario, a typical inverter topology with half-bridges operating at high switching frequencies and high blocking voltages limits the ability to measure these parameters online. This is increasingly important with the introduction of dynamic AC PCTs [4], operating the devices under test (DUTs) under application-oriented conditions.

Experimental Details

Fig. 1 shows the simplified equivalent circuit of a conventional static DC PCT for a MOSFET, with the typical injected power and temperature profile during the test. To induce thermomechanical stress in the DUT, it is repeatedly heated up and cooled down. Closing the control switch applies the heating current across the device during the heating phase (ton), therefore increasing the junction temperature. During the subsequent cooling phase (toff), the control switch is opened, allowing the DUT to cool down.

Fig. 2 shows the equivalent circuit of a typical H-bridge setup using two MOSFET half-bridges. The load inductor L reduces the current ripple during the test and varies depending on the nominal blocking voltage of the DUT. This dynamic APC method can subject the DUT to arbitrary current waveforms. It is possible to run a test with a DC current, similar to the conventional test, by using the load half-bridge as a buck converter while using only one of the DUT transistors. Such a dynamic PCT enables test conditions resembling the operating points in the field, revealing nonidealities in the operation of wide-bandgap devices like SiC MOSFETs or GaN HEMTs. Both the bias temperature instability of SiC MOSFETs [5] and the dynamic on-state resistance RDS,on of GaN HEMTs [6] are parasitic effects whose severity depends on the dynamic conditions that the devices are exposed to.

Fig. 3 shows a picture of the designed measurement board with the proposed TSEP acquisition circuits. This prototype board has a size of 41 x 130 mm and is designed to fit two boards next to each other on a full SiC module of the type BSM120D12P2C005. In addition to the acquisition circuits, the board is fitted with a microcontroller unit (MCU) board responsible for measuring and buffering the outputs of the circuits. The board connects to the gate drive circuit and power transistor. A central supply unit powers each board through an RJ-45 connector and two isolated DC/DC converters with low isolation capacitance for optimized common-mode rejection ratio (CMRR) performance. To increase the noise immunity, the acquired parameters are sent in a data package as a differential digital signal over the isolation barrier to a host PC. To measure multiple transistors at the same time, several measurement boards can be daisy-chained.

Results and discussion

To validate the simultaneous TSEP acquisition, an H-bridge test bench is operated in buck-converter configuration. A DC link voltage of 400 V is applied to the inverter, while the load current is regulated to a value of 50 A. The averaging count of the MCU is set to 100, resulting in a sample rate of 200 Sa/s of the acquired parameters for a PWM frequency of 20 kHz.

Fig. 4 shows a measurement of the quasi-threshold voltage with the gate-source voltage waveform overlayed with the voltage drop over the parasitic source inductance. The gate-source voltage waveform shows a ringing, that corresponds to the frequency of the voltage drop over the parasitic inductance waveform and for the most part is a measurement artifact owed to the finite CMRR of the used 100 MHz differential probe. The point at which the quasi-threshold voltage is detected is marked with a vertical dashed line. As soon as the threshold for the comparator is reached, the output of the flip-flop turns...
from a logical 0 to a logical 1 and signifies the point at which the gate-source voltage should be acquired. In this case, with a threshold of $V_{SS}$ of 200 mV, a $V_{th,q}$ of 5.8 V is measured.

Fig. 5 shows the measurement results for peak external gate resistance voltage during a switching cycle. The measured voltage is converted into the gate current with an external gate resistance of 4.7 $\Omega$. The external gate resistance voltage waveform shows a turn-on of the power MOSFET by a peak and a turn-off by a valley in the waveform. The peak external gate resistance voltage is acquired with the peak detector and a steady-state value of 3 A is set. Comparing the output of the acquisition circuit to the external gate resistance voltage waveform acquired with a 1 GHz differential probe, shows a deviation of 150 mA. Compared to the acquisition of the quasi-threshold voltage, the conversion of the peak gate current into a digital value has a lower demand on the acquisition delay, as the output is held by the peak detector.

The analog voltages at the output of the acquisition circuits are turned into robust digital signals through the MCU and passed through a galvanic isolation barrier for subsequent signal processing and temperature estimation by the host PC.

Conclusions
This work presents a test bench for online monitoring of electrical parameters of SiC power transistors during inverter operation. The technique can be adopted for state-of-health monitoring and EOL detection in wide bandgap power semiconductor devices and modules.

Acknowledgments
This work receives funding in the frame of the KDT JU project Archimedes under BMBF grant number 16MEE0326.

References